qaqadu events

Short courses are developed and presented by

steepest ascent

www.steepestascent.com

Technical Training 2012

DSP & Communication Theory Short Courses

DSP Theory, Architectures & Algorithms	3 Day	April 17-19 May 1-3 September 25-27 November 6-8	Munich, DE Scotland, UK Scotland, UK Munich, DE
Adaptive Filtering & Linear Algebra DSP	3 Day	March 20-22 October 2-4 on request	Scotland, UK Scotland, UK Munich, DE
Digital Communications	3 Day	March 6-8 November 27-29 on request	Scotland, UK Scotland, UK Munich, DE
Synchronisation for Digital Receivers	3 Day	February 21-23 on request	Scotland, UK Munich, DE
OFDM for Wireless Communications	3 Day	February 27-29 on request	Scotland, UK Munich, DE
MIMO for Wireless Communications	2 Day	April 2-3 September 11-12 on request	Scotland, UK Scotland, UK Munich, DE
DSP for FPGAs	3 Day	April 24-26 May 22-24 October 9-11 November 13-15	Scotland, UK Munich, DE Munich, DE Scotland, UK
FPGAs and Embedded Processors	3 Day	on request	Munich, DE Scotland, UK
Adaptive QR Algorithm Masterclass	2 Day	February 1-2 on request	Scotland, UK Munich, DE

Wireless Standards Short Courses

LTE & LTE Advanced Physical Layer	3 Day	March 27-29 on request	Scotland, UK Munich, DE
3GPP LTE Physical Layer	3 Day	on request	Munich, DE Scotland, UK
3GPP UMTS FDD Physical Layer	2 Day	on request	Munich, DE Scotland, UK
DVB-H	1 Day	on request	Munich, DE Scotland, UK
802.16 Physical Layer	2 Day	on request	Munich, DE Scotland, UK
Wireless / Mobile Channel Modelling	2 Day	September 4-5 on request	Scotland, UK Munich, DE
Wireless "Whitespace" Communications Design	2 Day	June 12-13 on request	Scotland, UK Munich, DE

DSP Implementation Short Course

VHDL Simulation and Synthesis	4 Day	February 7-10 on request	Scotland, UK Munich, DE
Channel Coding	3 Day	September 18-20 on request	Scotland, UK Munich, DE

Automotive Electronics

MOST Forum	1 Day	March 20	Stuttgart/Esslingen, DE

qaqadu event gmbh
Maximilianstraße 8
82319 Starnberg, Germany
T +49 8151 55 50 09 11
F +49 8151 55 50 09 10
E contact@qaqadu.com

Geschäftsführung:
Mandy Ahlendorf, Joachim Hüggenberg
HRB 173924, Amtsgericht München
TAX No. 117/135/50029 ID DE260317785
www.hightech-events.com

Kreissparkasse München Starnberg
Account 27007814 BLZ 702 501 50
IBAN DE67702501500027007814
SWIFT-BIC BYLADEM1KMS

DSP Theory, Architectures & Algorithms

SYLLABUS

Signal Processing Review

- Signals, systems and applications
- Amplification, distortion and noise
- The 90s DSP revolution to software radio today
- SFDR - Spurious free dynamic range

The Generic DSP System

- ADCs, DACs and signal conditioning
- Antialias and reconstruction filters
- Quantisation
- Noise and distortion
- The Nyquist sampling rate
- Undersampling techniques

Transform Domain Analysis

- Elementary signals
- Continuous time and discrete time signals
- Linear systems
- Convolution
- z-domain system representation
- z-domain system analysis

Frequency Domain Analysis

- Response of linear systems to sinusoids
- Periodic, aperiodic and random signals
- The Discrete Fourier Transform (DFT)
- The Fast Fourier Transform (FFT)
- Spectral leakage and windowing
- Time/frequency representation
- Danielson-Lanczos lemma
- Cooley-Tuckey algorithm
- Other FFT algorithms

Digital Filtering

- Finite Impulse Response (FIR) filters
- The “intuitive” digital filter
- Digital filter design parameters and methods
- Linear and non-linear phase
- Minimum and non-minimum phase
- Infinite Impulse Response (IIR) digital filters
- IIR filter stability
- z-domain poles and zeroes
- Bit true/fixed point implementation

Adaptive DSP Algorithms

- The generic adaptive filter
- Adaptive filter architectures
- Least squares minimisation
- Least Mean Squares (LMS) algorithm
- Channel equalisation / inverse system identification
- Feedback suppression
- Acoustic echo control / noise control
- RLS and QR algorithms

DSP Baseband Processing

- Decimation and interpolation techniques
- Filter banks
- Polyphase implementation
- Oversampling techniques
- Quantisation noise shaping
- Sigma delta ADCs/DACs

Digital Communications

- Information theory
- AM/FM/PM modulation
- ASK/PSK/FSK digital signalling
- Pulse shaping and matched filtering
- Raised cosine and root raised cosine filters
- QPSK and QAM digital communications
- Signal constellations
- Other modulation techniques
- Data equalisation
- Error control and coding

DSP for Mobile and Wireless

- Time/frequency/code division multiple access
- Spread spectrum modulation
- CDMA scrambling and channelisation
- Single carrier vs multicarrier
- Introduction to OFDM
- Channel modelling

DSP (Software) Enabled Radio Architectures

- Undersampling strategies
- Direct digital downconverters (DDC)
- f2/4 based systems
- Bandpass sigma delta
- QAM (Quadrature Amplitude Modulation)
- NCO (Numerically Controlled Oscillators)
- Synchronisation

DSP on FPGAs

- Overview of today’s FPGA technology
- Integer, floating point and fixedpoint arithmetic
- Multiply, divide and square root implementation
- Digital filter implementation
- Retiming and pipelining techniques

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

Adaptive Filtering & Linear Algebra

SYLLABUS

Review: Signal Processing Review
- Signal, systems and applications
- Linear Algebra/Matrix DSP systems

Review: Matrix Methods
- Matrices and linear algebra
- Matrix additions and multiplies
- Vectors
- Row and Column vectors
- Transpose matrices
- Complex matrices
- Hermitian transpose

Matrix properties
- The identity matrix
- Symmetric matrices
- Diagonal matrices
- Triangular matrices (upper and lower)
- Positive definite matrices
- Condition numbers
- Orthogonal Matrices
- Matrix inverse

Defining DSP Systems with Matrices
- FIR and IIR filters
- The DFT and IDFT
- OFDM Implementations
- Farrow filters for resampling
- Covariance matrices and properties
- Adaptive Filters
- Interleaving
- Hadamard matrices
- MIMO implementations / Smart Antennas
- Adaptive beamforming

Adaptive Filters
- Overdetermined system
- The method of least squares (pseudoinverse)
- The Wiener Hopf solution
- Gradient based methods
- Least mean square (LMS) methods
- Recursive least squares (RLS)
- RLS versus LMS
- Kalman implementations

Adaptive DSP Applications
- System Identification
- Inverse System Identification
- Noise cancellation
- Predictive Systems
- Multichannel systems
- Oversampling DSP systems

Complex Arithmetic Adaptive Systems
- The basic QAM RF system and baseband model
- Complex FIR filters for baseband IQ modelling
- Complex adaptive FIR Filters
- Complex arithmetic requirements
- Working with complex matrices

Linear Systems of Equations
- Simultaneous equations
- Linear set of equations
- Solution by Gaussian elimination
- Gaussian elimination with pivoting
- Underdetermined sets of equations
- Overdetermined sets of equations
- LU Decomposition
- Cholesky (LL^T Decomposition)
- Eigenvalue decomposition
- Singular value decomposition (SVD)

Matrix Inverse Methods
- Square sets of simultaneous equations
- Defining and calculating the matrix inverse
- Inverse of a diagonal matrix
- Method of backsubstitution
- Inverse of a triangular matrix and LU decomposition
- Practical Implementation on DSP processors

The QR Algorithm
- The QR Decompositions
- Orthogonality of Q; Upper Triangular nature of R
- Relation to Cholesky decomposition
- Householder decomposition
- Givens rotation based decomposition
- Systolic / parallel array for Givens based QR
- Solving linear sets of equations

QR/Cholesky Applications Smart Antenna
- High speed adaptive filters
- Adaptive least squares equalisation
- Adaptive beamforming methods
- Smart Antennas
- MIMO (multiply in-multiple out)
- Processing speed requirements

Real Time Arithmetic Requirements
- Overflow and underflow issues
- Multiply and addition requirements
- Floating point and fixed point implementations
- How many bits? (... certainly more than 16!)
- Square root and divide in QR
- *"Square root free"* methods for QR
- Using CORDIC to calculate sine and cosine
- Numerical integrity and round off noise
- Wordlength requirements
- Floating point implementations and issues
- DSP processors versus FPGAs.

Case Studies
- Baseband RF Channel Identification
- Baseband Acoustic System Identification
- QR using FPGA logic
- Complex channel equalisation
- FPGA implementation of Adaptive Systems
- QR arithmetic implementation using CORDIC
- Backsubstitution on co-processors
- MIMO Channel modelling, 802.11n, 3G SCM

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK, +44 (0)141 5528855, info@steepestascent.com
www.steepestascent.com

Digital Communications (3 DAY COURSE)

SYLLABUS

DSP Theory Review

- ADCs and DACs / signal conditioning
- Antialias and reconstruction filters
- Distortion, quantisation error and noise
- The Nyquist sampling rate
- z-domain representation and transforms
- FIR and IIR Digital Filters
- Poles and zeroes and the Z-domain
- Linear/non-linear phase
- Minimum/non-minimum phase

Single Carrier Data Communications

- Information theory
- AM/FM/PM modulation
- ASK/PSK/FSK signalling
- Complex signal representations
- Symbol constellations
- QPSK and QAM digital communications
- Pulse shaping
- Matched filtering techniques
- Inter-Symbol Interference (ISI)
- Orthogonal carrier principles
- Data equalisation

Adaptive DSP for Communications

- Adaptive applications (equalisation, beamforming)
- Adaptive architectures
- LMS Algorithm
- Non-canonical LMS algorithms
- RLS and QR algorithms
- Decision Feedback Equalisation
- Fractionally spaced equalisers
- Blind equalisation

Spread Spectrum Communications

- Time/frequency/code DMA (TDMA/FDMA/CDMA)
- Spread spectrum techniques
- Coding gain
- Direct sequence CDMA
- Multiple access interference
- PRBS sequence generation
- OVSF- orthogonal variable spreading function
- Walsh codes and multipath
- The near far problem
- Power control
- The rake receiver

OFDM Communications

- Historical perspective: DMT
- Motivation for multi-carrier vs single-carrier
- Introduction to OFDM
- The structure of an OFDM signal
- Sub-carrier symbol structure
- Generation of OFDM symbols using the IFFT
- Cyclic prefix (guard interval)
- OFDM signal bandwidth
- OFDM dynamic range considerations
- Peak-to-average power ratio (PAR)
- Crest factor measurements and limits
- RF Amplifier clipping considerations
- Minimising / reducing PAR
- SC-FDMA

Propagation Channels

- Time & frequency channel dispersion
- AWGN and Multipath Propagation Channels
- Delay Spread Values and Time Variations
- Loss of orthogonality in CDMA signals
- Loss of orthogonality in OFDM signals
- Fast and slow fading environments
- Complex baseband multipath channels

Single Carrier Synchronisation

- Optimal receiver structure
- Maximum Likelihood parameter estimation
- Phase and frequency recovery
- Phase Locked Loops (PLLs)
- The Costas loop
- Squaring Loops
- Numerically Controlled Oscillators
- Symbol recovery
- Equalisation techniques
- Error Vector Magnitude (EVM) measurements

OFDM Synchronisation

- Inter-Carrier Interference (ICI)
- Sensitivity to synchronisation errors
- Symbol timing recovery
- Carrier frequency recovery
- Frequency domain equalisation
- Use of training symbols and the cyclic prefix
- Frame Synchronisation

MIMO

- Spectral efficiency and capacity
- Transmit and receive diversity
- The Alamouti Scheme
- Delay Diversity and Cyclic Delay Diversity
- Beamforming
- Spatial multiplexing
- Singular Value Decomposition
- Equalising and predistortion in MIMO systems
- Precoding and combining in MIMO systems
- Codebooks for MIMO

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

Synchronisation

SYLLABUS

Single Carrier Modulation Review

- Amplitude, Frequency and Phase Shift Keying
- Quadrature Amplitude Modulation
- Complex Representation of QAM
- Constellation Diagrams
- Pulse Shaping
- Matched Filtering
- Effect of Synchronisation Errors
- Inter-Symbol Interference
- Eye Diagrams

Single Carrier Synchronisation

- Maximum Likelihood Parameters Estimation
- Open Loop Techniques
- Closed Loop Techniques
- Carrier Frequency Recovery
- Band Edge Filtering
- Carrier Phase Recovery
- Phase Locked Loops (PLLs)
- Squaring Loops
- Costas Loops
- Symbol Timing Recovery
- Delay Locked Loops (DLLs)
- Coherent and Non-Coherent Techniques
- Decision Directed Techniques
- Non-Decision Directed Techniques
- Signal Acquisition
- Frame Synchronisation
- Exploiting Pilot Symbols

Signal Resampling

- Multi-Rate DSP Review
- Decimation
- Interpolation
- Resampling by Non-Integer Factors
- Polyphase Filter Decomposition
- Polyphase Implementation
- Sinc Interpolation
- Variable Delay FIR Filter
- Farrow FIR Structure

Propagation Channels

- Additive White Gaussian Noise Channels
- Multipath Propagation
- Delay Spread
- Coherence Bandwidth
- Coherence Time
- Fading Environments
- Baseband Channel Modelling

Direct Sequence Spread Spectrum Synchronisation

- Direct Sequence Spread Spectrum Review
- Channelisation and Scrambling
- Spreading Gain
- Pilot Channels
- Multipath Resolution
- Channel Estimation
- Delay-Locked Loops
- RAKE Receiver Structure

OFDM Synchronisation

- OFDM Signal Structure
- OFDM Modulation using the IFFT
- Cyclic Prefix / Guard Interval
- Bandwidth Control through Windowing
- Oversampling
- Sensitivity to Synchronisation Errors
- Inter-Carrier Interference
- Carrier Frequency Offset
- Symbol Timing Recovery
- Frequency Domain Equalization
- Effects of Phase Noise
- Exploiting the Cyclic Prefix
- Utilising OFDM Pilot Sub-Carriers

Equalisation

- Adaptive Filtering
- Linear Equalisation
- Decision Feedback Equalisers
- Fractionally Spaced Equalisers
- The Viterbi Equaliser

Case Studies:

- *3G (WCDMA)*
- Initial Timing Synchronisation Procedure
- Timing Refinement using DLLs
- Coherent Demodulation using Continual Pilot

- *Bluetooth (GFSK / DQPSK)*
- Signal Acquisition
- Preamble Correlation
- Frequency Recovery
- Timing Recovery

- *Wi-Fi 802.11 (OFDM)*
- Structure of Training Symbols
- Signal Acquisition
- Coarse and Fine Frequency Estimate
- Channel Estimation
- Frequency Tracking

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

OFDM for Wireless Communications

SYLLABUS

DSP Theory Review

- Sampling
- Anti-alias and reconstructions filters
- z-domain representation and transforms
- FIR and IIR Digital Filters
- Poles and zeroes and the Z-domain
- Linear/non-linear phase
- Minimum/non-minimum phase

Single Carrier Modulation Review

- Single Carrier: Transmit & Receive
- Quadrature amplitude modulation (QAM)
- Symbol Mapping: from QPSK to 256-QAM
- Pulse shaping techniques (RRC)
- Matched filtering techniques
- Channel noise and other imperfections
- QAM - Complex Arithmetic Representations
- Complex baseband multipath channels
- Time & frequency channel dispersion
- Inter-Symbol Interference (ISI)
- Orthogonal carrier principles

DSP OFDM Components

- The generic wireless communication system
- The Discrete Fourier Transform (DFT)
- The Fast Fourier Transform (FFT)
- The inverse FFT (IFFT)
- Windowing for FFTs
- Danielson-Lanczos lemma
- Cooley-Tuckey algorithm
- Other FFT algorithms

OFDM Principles

- Historical perspective: DMT
- Motivation for multi-carrier vs single-carrier
- Introduction to OFDM
- The structure of an OFDM signal
- Sub-carrier symbol structure
- Generation of OFDM symbols using the IFFT
- Cyclic prefix (guard interval)
- OFDM signal bandwidth

Practical Issues with OFDM

- Multipath interference on an OFDM symbol
- Protecting against multipath using cyclic prefix
- Reducing bandwidth (windowing vs filtering)
- Oversampling strategies
- The use of channel coding COFDM
- Generic OFDM transmitter structure

Power Considerations

- OFDM dynamic range considerations
- Peak-to-average power ratio (PAR)
- Crest factor measurements and limits
- RF Amplifier clipping considerations
- Intermodulation components
- General out of band power generation
- Minimising / reducing PAR
- SC-FDMA

Propagation Channels

- AWGN and Multipath Propagation Channels
- Delay Spread Values and Time Variations
- Loss of orthogonality in OFDM signals
- Fast and slow fading environments

Single Carrier Synchronisation and Receiver Design

- Optimal receiver structure
- Maximum Likelihood parameter estimation
- Phase and frequency recovery
- Symbol recovery
- Equalisation techniques
- Error Vector Magnitude (EVM) measurements

OFDM Receiver Design

- Inter-Carrier Interference (ICI)
- Carrier frequency offset
- Sensitivity to timing errors
- Symbol timing recovery
- Frequency domain equalisers (subcarrier)
- Effects of phase noise
- Synchronisation using training symbols
- Synchronisation using cyclic extension

Advanced and Emerging OFDM Architectures

- Beamforming strategies for OFDM
- Flash-OFDM
- MIMO techniques for OFDM
- Multicarrier CDMA (MC-CDMA)
- Frequency hopping OFDMA
- OFDMA vs MC-CDMA

OFDM based Standards

- 3GPP Long Term Evolution (LTE)
- LTE E-UTRA: DL OFDMA and UL SC-FDMA
- 802.11 - Physical Layer and MAC
- 802.16 - Physical Layer and MAC
- WiMax and 802.16e
- 802.20: Mobile Broadband Wireless Access (MBWA)
- 802.20: FDD and TDD Proposals

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

SYLLABUS

Introduction to Multi-antenna Systems

- Motivation
- Types of multi-antenna systems
- MIMO vs. multi-antenna systems

Diversity

- Exploiting multipath diversity
- Transmit diversity
- Space-time codes
- The Alamouti scheme
- Delay diversity
- Cyclic delay diversity
- Space-frequency codes
- Receive diversity
- The rake receiver
- Combining techniques

Spatial Multiplexing

- Spectral efficiency and capacity
- Transmitting independent streams in parallel
- Mathematical notation
- The generic MIMO problem
- Singular Value Decomposition
- Eigenvalues and eigenvectors
- Equalising MIMO systems
- Disadvantages of equalising MIMO systems
- Predistortion in MIMO systems
- Disadvantages of predistortion in MIMO systems
- Precoding and combining in MIMO systems
- Advantages of precoding and combining
- Disadvantages of precoding and combining
- Channel state information
- Codebooks for MIMO

Beamforming

- Beamforming principles
- Increased spectrum efficiency
- Interference cancellation
- Switched beam beamformer
- Adaptive beamformer
- Narrowband beamformer
- Wideband beamformer

Case study: MIMO in LTE

- Codewords to layers mapping
- Precoding for spatial multiplexing
- Precoding for transmit diversity
- Beamforming in LTE
- Cyclic delay diversity based precoding
- Precoding codebooks

Propagation Channels

- Time & frequency channel dispersion
- AWGN and multipath propagation channels
- Delay spread values and time variations
- Fast and slow fading environments
- Complex baseband multipath channels
- Narrowband and wideband channels
- MIMO channel models

Channel Estimation

- Channel estimation techniques
- Estimation and tracking
- Training based channel estimation
- Blind channel estimation
- Channel estimation architectures
- Iterative channel estimation
- MMSE channel estimation
- Correlative channel sounding
- Channel estimation in single carrier systems
- Channel estimation for CDMA
- Channel estimation for OFDM

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

DSP for FPGAs

SYLLABUS

Introduction to DSP FPGA Hardware

- From discrete logic to FPGAs -some history!
- The generic DSP system
- DSP cores and processors review
- Custom and semi-custom ASICs
- System-on-chip (SOC)
- FPGA flexibility and functionality
- FPGAs vs Programmable DSPs

Linear Systems DSP Algorithm Review

- Aliasing and reconstruction filters
- Sampling rates and wordlengths
- Z-domain notation and fundamental analysis
- Frequency domain analysis
- Finite Impulse Response (FIR) filters
- Infinite Impulse Response (IIR) filters
- Digital filter design and specification
- Oversampling techniques (sigma delta)

FPGA Technology

- The FPGA technology roadmap
- Clocking rates, data rates and sample rates
- FPGA memory and registers
- Input/output blocks and requirements
- Bits, Slices and Configurable Logic Blocks
- Comparable MIPs Performance Ratings
- FPGA Families and Sources

FPGA elements for DSP algorithms

- Building delay lines and Shift Registers
- Use of RAM (memory) on FPGAs
- Serial to Parallel and Parallel to serial
- Multiplexors for channel selection
- Full adders, carry logic, and adder trees
- Multipliers: Shift and Add; ROM based
- Efficient multiplier implementation

DSP Arithmetic Essentials

- 2's complement fixed point arithmetic
- Fundamental adders and multiplier arrays
- Division and square root arrays....not so easy!
- Wordlength issues & Fixed point arithmetic
- Saturate and wraparound
- Overflow and underflow
- CORDIC techniques
- Complex arithmetic requirements

Signal Flow Graph (SFG) Techniques

- DSP/Digital Filter Signal Flow Graphs
- Latency, delays and "anti-delays"!
- Re-timing: Cut-set and delay scaling
- The transpose FIR
- Pipelining and multichannel architectures
- SFG topologies for FPGAs

Frequency Domain Processing

- Discrete Fourier Transform (DFT) Review
- Fast Fourier Transform (FFT)
- The FFT and IFFT
- FFT FPGA architectures
- FFT wordlength growth and accuracy

Digital Filtering for FPGAs

- Symmetric / Linear Phase Filters
- Upsampling and interpolation filters
- Downsampling and decimation filters
- Efficient arithmetic for FIR implementation
- Integrators and differentiators
- Half-band, moving average and comb filters
- Cascade Integrator Comb (CIC) Filters (Hogenauer)
- Efficient arithmetic for IIR Filtering

Adaptive DSP Algorithms and Applications

- Adaptive applications (equalisation, beamforming)
- LMS Algorithms and parallel implementation
- Non-canonical LMS algorithms
- Linear algebra; solving linear systems of equations
- The QR algorithm for adaptive signal processing
- QR processing requirements and numerical issues

DSP Enabled Communications & FPGAs

- Quaternary Phase Shift Keying (QPSK)
- Transmit/Receive Filters - Root Raised Cosine
- Undersampling & Digital Downconversion
- Direct digital upconversion
- Digital IF stages (and fs/4 Systems)
- Numerically controlled oscillators (NCO)
- Channel coding requirements
- Design partitioning for FPGAs

Timing and Sychronisation Issues

- Carrier recovery, squaring & Costas loops, PLLs
- Phase rotations; Sampling rate conversions
- Symbol timing recovery, early/late gate detection
- Multirate and polyphase filters
- Delay locked loop timing and synchronisation

Embedded Processors for FPGAs

- Embedded systems
- System-on-chip design methodologies & flows
- On-chip network topologies and standards
- System profiling and hardware acceleration
- Xilinx Platform Studio (XPS)
- PicoBlaze, MicroBlaze embedded processors
- DSP algorithms on embedded processors

LABORATORY SESSIONS

The laboratory sessions for this course will be based upon the Xilinx DSP design flows. System Generator for Matlab/Simulink, Xilinx ISE and XPS software tools will be used to design DSP systems for the Xilinx XUP development kit.

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

FPGAs and Embedded Processors

SYLLABUS

Introduction to FPGAs

- From discrete logic to FPGAs- some history
- FPGA flexibility and functionality
- FPGAs vs Programmable DSPs
- The FPGA technology roadmap

FPGA Technology

- Clocking rates, data rates and sample rates
- Slices and Configurable Logic Blocks
- Input / output blocks
- FPGA memory and registers
- DSP processing blocks
- Comparable MIPs performance ratings
- FPGA Families

Digital Signal Processing and FPGAs

- Linear systems DSP algorithm review
- FPGA elements for DSP algorithms
- DSP arithmetic essentials
- Signal Flow Graph (SFG) techniques
- Digital filtering for FPGAs

Introduction to Embedded Systems

- Embedded system overview
- Embedded system design flows
- Real Time Operating Systems (RTOS)
- Embedded system debugging techniques

System-on-Chip

- Design methodologies & flows
- Intellectual Property (IP) Cores
- On-chip network topologies
- On-chip network standards
- FPGAs as a System-on-Chip platform

FPGA Embedded Processors

- Xilinx® PicoBlaze™ overview
- Xilinx MicroBlaze™ overview
- Xilinx PowerPC® overview
- Altera® Nios® II overview
- ARM® Cortex™-M1 overview

Xilinx Embedded Tool Environment

- Xilinx Embedded Design Flow
- Xilinx Platform Studio (XPS)
- XPS Software Development Kit (SDK)
- Xilinx System Generator for DSP
- Xilinx ChipScope™ Pro

FPGA Embedded Processor Systems

- Interfacing IP Cores to Embedded Processors
- FPGA hardware and software debug
- System performance profiling
- Software acceleration using Co-Processors

LABORATORY SESSIONS

The laboratory sessions for this course will be based upon the Xilinx Embedded and DSP design flows. Xilinx XPS, ISE™ and System Generator for DSP software tools will be used to design Embedded DSP systems for the Xilinx XUP development kit.

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

Adaptive QR Algorithm Masterclass

SYLLABUS

In this masterclass we will present the QR algorithm and explicitly look at why and where it is now extensively used in DSP and Digital Communications in applications such as MIMO, equalisers, and beamformers. The QR algorithm is widely known and used in linear and matrix algebra to decompose a matrix into an orthogonal matrix, Q, and upper triangular matrix R. As such the algorithm is used for finding the solution of a linear set of equations, or expressed in matrix algebra, for implicitly solving for a vector, w = R-1p. without explicitly forming a matrix inverse, which in fixed point arithmetic may be an ill-conditioned problem, and suffer from overflow/underflow: In this course we will review algorithm, applications and real FPGA implementations.

The course will include:

- Matrix Algebra Review
- QR History - Classical Linear Algebra
- Householder and Givens transforms
- Least Squares DSP Implementations
- Fixed point implementations
- Parallel and Serial FPGA Implementations
- Backsubstitution versus Downdating Arrays
- CORDIC and Arithmetic Requirements
- Singular Value Decomposition (SVD)
- Beamforming and Beamsteering
- MIMO System Implementation
- Fixed point implementations

SYLLABUS

This workshop brings together two industry leaders to provide unique and unrivalled insight into the LTE radio interface. In so doing, it examines key LTE radio interface procedures and protocols. Lab sessions enable students to encode RRC ASN.1 messages in a practical manner putting to practice key parameters. The workshop examines LTE physical layer in detail, using various demo and practical lab sessions to demystify Physical Channel mapping, Hybrid ARQ operation and Downlink Channel Estimation. Unique to our offering is the blend of theoretical course and hands-on software simulation modelling. No experience required.

Who Should Attend
Engineers and managers involved in design and testing of the LTE Radio Interface. Personnel who desire a comprehensive explanation of the LTE Radio Interface.

Course Outline
Divided into 10 sections, the topics covered will include:

Section 1: Introducing LTE (1 hour)

- 3GPP Evolution, From R5 to R10, the goals of LTE.
- Review of the LTE Architecture, E-UTRAN, E-UTRA, eNB and E-UTRAN interfaces, EPC, MME, S-GW, PDN Gateway, SGSN, IMS.
- User Equipment functionality and Identities, IMSI, GUTI, M-TMSI, S-TMSI and C-RNTI.
- Network Identities, TAI (Tracking Area Identity) and Cell Identity.
- LTE performance
- Spectrum and Channel Bandwidths Options.

Section 2: Review of the LTE Physical Layer (1.5 hours)

- Services provided by the Physical Layer.
- E-UTRA Physical Layer, overview of OFDMA and SC-FDMA, subcarriers, OFDM symbols, cyclic prefix, Physical Resource Block.
- LTE generic frame structure, slots and subframes, frequency bands, carrier frequencies and EARFCN.
- The LTE downlink physical channels - PBCH, PCFICH, PDCCH, PHICH, Synchronization and Reference Signals.
- The LTE uplink physical channels - PRACH, PUCCH, PUSCH, uplink reference signals.
- Modulation and Coding, QPSK, 16QAM, 64QAM, Turbo Coding.

Section 3: LTE Air Interface Protocols (3.5 hours)

- Defined the use of NAS, IP, RRC, PDCP, RLC and MAC.
- The E-UTRA Interface, Stratums, NAS Control Plane, NAS User Plane, NAS Messages, EMM Messages and ESM Messages.
- LTE States, EPS Mobility Management States, EMM States in the UE, EMM States in the MME, EPS Connection Management States.
- The E-UTRA Protocols, Radio Resource Control, RRC Messages, RRC States, Establishment of an RRC Connection.
- PDCP services and functions, PDCP profiles, compression standards, PDCP headers and frame formats.
- RLC, RLC Transparent Mode, RLC Unacknowledged Mode and RLC Acknowledged Mode, RLC PDUs, the TMD PDU, UMD PDU, AMD PDU, AMD Segment PDU and the RLC Status PDU.
- MAC functions and operation.
- Logical Channels - BCCH, PCCH, CCCH, DCCH, DTCH.
- Transport Channels - BCH, DL-SCH, PCH, UL-SCH, RACH.
- Mapping Logical Channels into Transport Channels - RNTI Identities, random access process, non-contention based random access procedure.

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

SYLLABUS

Section 4: LTE Operational Procedures (2.5 hours)

- Contents of RRC MIB and SIB messages, Scheduling Options.
- PLMN selection and Initial Cell Selection algorithms, Optimization of Parameters.
- LTE initial procedures, RRC Connection, Signalling Radio Bearers.
- Attach, PDN connectivity and Default and Dedicated Bearer Establishment.
- RRC UE Capability and Security.
- RRC Messages in operation.
- SON Architecture and Automatic Neighbour Relationship procedures.
- E-UTRA and LTE Security - authentication, algorithms and keys, ciphering and integrity.
- End to End Downlink and Uplink IP Data Flow.

Section 5: LTE Mobility (1 hour)

- LTE mobility, LTE cell planning, capacity and coverage planning, frequency deployment options.
- Soft Frequency Re-use Options.
- Mobility functional architecture, role of the eNB and MME, Tracking Areas.
- Idle Mode procedures, LTE Idle Mode monitoring requirements.
- E-UTRA Measurements, RSSI, RSRP, RSRQ.
- Cell reselection, intra-frequency measurements, inter-frequency and inter-RAT measurements, high and medium mobility states, ranking of cells, Tracking Area Update.
- Mobility in the LTE Active State, measurements and gap configurations, event triggers, timing, the handover process.
- EPC mobility (Relocation).
- Femto cells, scenarios and assumptions, HeNB selection.
- 3GPP interworking, E-UTRAN to UTRAN / GERAN RAU procedure, E-UTRAN to UTRAN / GERAN handover procedure.

Section 6: OFDM in LTE (1 hour)

- OFDM motivation: spectral efficiency, equalization, bandwidth flexibility, resilience to multipath.
- OFDM signal structure: subcarriers, orthogonality, the cyclic prefix, OFDM symbols, fundamental period.
- OFDM signal structure in LTE: the resource grid, resource elements, resource blocks, slots and subframes.
- Generation of OFDM signals using the IDFT, efficient implementation with IFFT.
- The cyclic prefix: OFDM signals and multipath, LTI system response, mobility, channel delay spread.
- OFDM windowing: out of band emissions reduction, windowing versus filtering versus EVM.
- Oversampling and upconversion of OFDM signals, baseband spectral occupancy, filtering considerations.
- Peak to average power ratio reduction techniques, clipping, peak windowing, peak cancellation.
- SC-FDMA: LTE uplink modulation, DFTS-OFDM, subcarrier mapping.

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

SYLLABUS

Section 7: LTE Multiplexing and Channel Coding (2 hours)

- Transport channels & control information: DL-SCH, PCH, BCH, DCI, CFI, HI, UL-SCH and UCI.
- Mapping of transport channels to physical channels.
- CRC coding, polynomials, CRC masking of DCI messages and BCH coding.
- Code block segmentation, filler bits, turbo coder block sizes, code block CRC attachment.
- Convolutional and turbo coding, tail biting, Quadratic Permutation Polynomial (QPP) interleaving.
- Rate matching, bit selection and pruning, subblock interleaving, role of HARQ.
- Transport channel and control information processing chains.
- HARQ in LTE, incremental redundancy, Chase combining, stop and wait processes.

Section 8: MIMO Review (1 hour)

- Motivation, increased capacity, increased robustness.
- Multiantenna systems classification, SISO, MISO, SIMO and MIMO. Beamforming, diversity, spatial multiplexing.
- Transmit and receive diversity, diversity gain.
- The Alamouti sheme, space time coding, space frequency coding, decoding procedure.
- Delay diversity and cyclic delay diversity (CDD), relationship with OFDM and multipath.
- Beamforming, SNR maximisation.
- Spatial multiplexing, narrowband assumption, channel matrix, channel rank, spatial streams and layers.
- Equalising and predistortion in MIMO systems, noise enhancement, advantages and disadvantages.
- Precoding and combining in MIMO: Singular value decomposition (SVD), codebook and non-codebook based precoding, signalling overhead.
- Codebook based precoding, desired codebook attributes, codebook selection, signalling overhead.

Section 9: Downlink Physical Channels and Signals (3 hours)

- Downlink physical channel processing chain, scrambling, modulation, layer mapping, precoding.
- Codewords and layers, antenna ports and physical antennas.
- Scrambling and modulation, PRBS initialisation, BPSK, QPSK, 16QAM and 64QAM constellations.
- Downlink multi-antenna processing, transmission schemes, layer mapping and precoding, transmit diversity, cyclic delay diversity (CDD), spatial multiplexing, beamforming.
- Cell identities. Cell identity group, identity within the group, mapping to cell search procedure.
- Synchronisation signals: PSS & SSS, structure, mapping to resource grid, timing acquisition, cell search.
- Reference signals: Cell specific, UE specific & MBSFN, reference signal antenna ports, channel estimation.
- Downlink physical channels: PBCH, PCFICH, PHICH, PDSCH & PDCCH, processing chains.
- The control region, Resource Element Groups (REGs), Control Channel Elements (CCEs), PDCCH search spaces, role of CFI.
- Mapping of physical channels and signals to the resource grid, relationship between antenna ports and physical antennas.
- Closed and open loop spatial multiplexing, precoding matrix selection, role of PMI and RI.
- Codebook based and non-codebook based beamforming in LTE.
- Transmit diversity, space frequency block coding matrices.

SYLLABUS

Section 10: Uplink Modulation (1 hour)

- Uplink physical channel processing chain, scrambling, modulation, SC-FDMA precoding.
- Scrambling and modulation, BPSK, QPSK, 16QAM and 64QAM constellations.
- SC-FDMA symbol construction, DFT sizes, uplink resource allocation size restrictions, subcarrier mapping.
- Uplink reference signals: DRS and SRS, uplink channel estimation problem, SRS structure and timing.
- Uplink physical channels: PUSCH, PUCCH & PRACH processing chains.
- Control information: Channel Quality Information (CQI), Rank Indication (RI), Precoding Matrix Indication (PMI), HARQ Indicator (HI), Scheduling Request (SR).
- Control signalling on PUSCH, data and control interleaving and multiplexing, ACK/NACK placeholder bits.
- Control signalling on PUCCH, PUCCH Formats 1, 1a, 1b, 2, 2a, 2b, PUCCH resources, cyclic shifts, resource element mapping.

Lab Sessions

The course contains a number of practical elements in the form of demonstrations and lab sessions. These include:

Lab Session 1: RRC Signalling Messages and Parameters (1.5 hours)

- Getting ASN.1 from 3GPP LTE RRC Specifications.
- ASN.1 Message Encoding.
- Encoding the MIB and SIB Messages.
- RRC Connection and Connection Setup Messages.

Lab Session 2: RRC Measurement Configuration (1 hour)

- Generating the RRC Connection Reconfiguration Message.
- Measurement Configuration Options.
- Encoding Intra and Inter LTE Mobility Parameters.

Lab Session 3: Mapping of Physical Channels to the Resource Grid (1 hour)

- Generating the resource grid.
- Generating physical channels and physical signals.
- Mapping to the resource grid.
- Effect of Cell Id.
- Effect of antenna port.

Lab Session 4: Hybrid ARQ for PDSCH (0.5 hour)

- PDSCH transmission and reception processing.
- Uncoded performance of QPSK, 16QAM and 64QAM.
- Coded performance without Hybrid ARQ.
- Coded performance improvement with Hybrid ARQ.

Lab Session 5: Downlink Channel Estimation (1.5 hour)

- Channel estimation using DRS.
- Interpolation of estimates.
- Resource grid edge effects.
- Effect of channel conditions in estimates.
- Received signal equalisation.

SYLLABUS

Demo 1: LTE OFDM Transmission Mask (0.5 hour)

- Transmission mask specifications.
- Windowing effects.
- Additional filtering requirements.

Demo 2: MIMO in LTE (0.5 hour)

- Beamforming radiation pattern examples.
- 2 and 4 antenna MIMO directional capability examples.

Demo 3: RRC Random Access (0.5 hour)

- Cell Random Access Options.
- SIB 2 Configuration Parameters.

3GPP LTE Physical Layer

SYLLABUS

Introduction to 3GPP Long Term Evolution

- Key LTE system parameters
- Harmonisation of LTE with WCDMA
- LTE Downlink: OFDMA
- LTE Uplink: SC-FDMA

LTE Physical Layer Modulation

- LTE Generic Frame Structure
- Downlink and uplink slot formats
- Resource elements & resource blocks
- Physical channels & signals
- Scrambling and modulation
- Mapping of symbols to physical resources
- Control channels and their system role

LTE Physical Layer Coding

- CRC coding
- Code block segmentation
- Convolutional and turbo coding
- Rate matching

Spectral Efficiency in LTE

- Hybrid-ARQ
- Multi-user scheduling
- Resource allocation
- Frequency reuse planning

OFDMA

- OFDMA basics
- Advantages over other techniques
- Examples of standards that use OFDMA
- Pitfalls of OFDMA

SC-FDMA

- Motivation for the use of SC-FDMA
- Localised SC-FDMA
- Interleaved SC-FDMA
- Peak to average power ratio of SC-FDMA
- SC-FDMA equalisation

MIMO

- Spectral efficiency and capacity
- Transmit and receive diversity
- The Alamouti Scheme
- Delay Diversity and Cyclic Delay Diversity
- Beamforming
- Spatial multiplexing
- Singular Value Decomposition
- Equalising and predistortion in MIMO systems
- Precoding and combining in MIMO systems
- Codebooks for MIMO

MIMO in LTE

- Codewords to layers mapping
- Precoding for spatial multiplexing
- Precoding for transmit diversity
- Beamforming in LTE
- Cyclic delay diversity based precoding
- Precoding codebooks

OFDM Communications Theory

- Motivation for multi-carrier vs single-carrier
- Introduction to OFDM
- The structure of an OFDM signal
- Sub-carrier symbol structure
- Generation of OFDM symbols using the IFFT
- Cyclic prefix (guard interval)

OFDM Practical Considerations

- Multipath interference on an OFDM symbol
- Windowing to reduce out of band emissions
- Oversampling and upconversion
- The use of channel coding COFDM
- Peak-to-average power ratio (PAR)
- Techniques for reducing PAR

OFDM Receiver Design

- Inter-Carrier Interference (ICI)
- Sensitivity to synchronisation errors
- Symbol timing recovery
- Carrier frequency recovery
- Frequency domain equalisation
- Use of training symbols and the cyclic prefix
- Frame synchronisation

WCDMA Review

- Direct sequence spread spectrum comms
- UMTS / WCDMA overview
- Frequency Division Duplex (FDD) mode
- High Speed Packet Access (HSPA)

Frequency Domain & The FFT

- Fourier Series Review
- The Discrete Fourier Transform (DFT)
- The Fast Fourier Transform (FFT)
- The Inverse FFT (IFFT)
- Spectral leakage
- Danielson-Lanczos lemma
- Cooley-Tuckey algorithm
- Other FFT algorithms

Single Carrier Communications Review

- Quadrature amplitude modulation (QAM)
- Pulse shaping & Matched filtering
- Inter-Symbol Interference (ISI)
- Orthogonal carrier principles

Propagation Channels

- Time & frequency channel dispersion
- AWGN and multipath propagation channels
- Delay spread values and time variations
- Fast and slow fading environments
- Complex baseband multipath channels
- Narrowband and wideband channels

steepest ascent
Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

3GPP UMTS FDD Physical Layer

SYLLABUS

Mobile Communication Generations

- 1st generation analog mobile
- 2nd generation mobile GSM
- 3rd generation UMTS, IMT2000
- 3G partnership project (3GPP)

Spread Spectrum Principles

- Time/frequency/code DMA (TDMA/FDMA/CDMA)
- Spread spectrum techniques
- Coding gain
- Direct sequence CDMA
- Multiple access interference
- PRBS sequence generation
- OVSF- orthogonal variable spreading function
- Walsh codes and multipath
- The near far problem
- Power control
- The rake receiver
- Multiuser detection

3GPP Frequency Division Duplex

- 3GPP standard organisation
- Uplink and downlink architectures
- Bits, chips, slots and radio frames

3GPP Baseband Processing

- CRC
- Convolutional/turbo coding
- Interleaving
- Rate matching
- Transport channel multiplexing
- Spreading (channelisation & scrambling)
- Uplink/downlink channelisation codes
- Uplink/downlink scrambling codes
- Pulse shaping
- Modulation

3GPP Channelisation and Scrambling

- Uplink spreading: one DPDCH
- Uplink spreading: multiple DPDCHs
- Uplink scrambling code generation
- Uplink channelisation codes
- Uplink spreading: HPSK modulation
- Downlink DPCH spreading
- Downlink scrambling code generation
- Downlink scrambling codes organisation
- Downlink channelisation codes

Physical Channels for 3GPP FDD

- Transport channels
- Mapping of transport channels into physical channels
- Uplink physical channels
- Downlink physical channels
- Cell search procedure
- Slot synchronisation
- Frame synchronisation
- Scrambling code identification

3G Evolution

- UMTS Release 5: HSDPA
- HSDPA architecture
- Fast user scheduling
- Fast hybrid -ARQ
- High speed transport channels
- High speed physical channels
- UMTS Release 6: HSUPA
- UMTS Release 8: Long term evolution (LTE)

Propagation Channels

- Time & frequency channel dispersion
- AWGN and Multipath Propagation Channels
- Delay Spread Values and Time Variations
- Loss of orthogonality in CDMA signals
- Fast and slow fading environments
- Complex baseband multipath channels

DSP Baseband Communications Review

- Noise in communication systems
- Pulse shaping / matched filtering
- Sigma delta and bandpass sigma delta
- Channel equalisation / inverse system identification

Modulation and Mixing Strategies

- AM/FM/PM modulation
- ASK/PSK/FSK signalling
- Quadrature amplitude modulation (QAM)
- Complex notation and representation

MORE DETAILS

Should you have any further questions about this or any other Steepest Ascent courses, or if you are interested in an on-site presentation please contact:

amreet@steepestascent.com

Tel: +44 (0)141 552 8855

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

SYLLABUS

DVB-T - Digital Video Broadcasting - Terrestrial

- Multiple Frequency Networks
- Single Frequency Networks
- Channel Coding
- Channel Modulation
- Supported Operating Modes
- OFDM Frame Structure
- Reference Signals
- Transmission Parameter Signalling
- Spectral Characteristics

Mobile TV Standard (Overview)

- Introduction to digital TV
- Media Flo
- T-DMB
- ISDB-T
- MBMS
- DVB-H+

DVB-H - Digital Video Broadcasting - Handheld

- Backward compatibility to DVB-T
- Additional operating modes
- Time slicing techniques for power saving
- Multiprotocol Encapsulation (MPE)
- MPE Forward Error Correction (MPE-FEC)
- Physical Layer additions - signalling & interleaving
- Frequency Domain Parameters for DVB-H
- Typical link budget
- DVB-H signal acquisition

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

802.16 Physical Layer

SYLLABUS

802.16 History

- What is 802.16?
- IEEE 802.16 task groups
- IEEE 802.16-2001, .16a and .16c overview
- IEEE 802.16-2004 overview
- Further 802.16 task groups
- What is WiMAX?
- Wireless HUMAN
- WirelessMAN-SC and SCa PHYs
- WirelessMAN-OFDM PHY

802.16-2004

- OFDMA symbol construction
- Subchannels and OFDMA slots
- Data regions and segments
- Permutation zones and modes
- PUSC and FUSC subcarrier permutations
- Adjacent subcarrier permutation
- OFDMA frame structure
- PUSC segmentation
- Frame Control Header
- Downlink and uplink map information

Introduction to OFDM

- Frequency selective fading challenges
- What's orthogonal about OFDM?
- The IDFT
- The cyclic prefix
- Windowing and oversampling
- OFDM Peak to Average Power Ratio
- Scrambling for PAPR reduction
- PAPR reduction error correction coding

802.16e

- The 802.16e standard
- Mobile WiMAX
- 802.16e PHY changes
- Compressed and reduced map messages
- Updated adaptive antenna system
- Revised space-time coding and handover
- MIMO midambles
- Pilot subcarriers for multiple antennas
- Data randomisation
- Symbol repetition
- Hybrid ARQ
- Low Density Parity Check (LDPC) code
- Improvements to power control

MIMO

- MIMO features
- Spectral efficiency and capacity
- Single-user versus multi-user
- The Alamouti scheme
- Delay diversity
- Narrowband versus wideband
- MIMO-OFDM

Synchronisation

- Carrier recovery
- Squaring & Costas loops
- PLLs
- Phase rotation
- Sampling rate conversion
- Symbol timing recovery
- Early/late gate detection
- Multirate and polyphase filters
- Delay locked loop timing and synchronisation
- Numerically controlled oscillators

OFDM Synchronisation

- Complex representation of OFDM symbols
- OFDM receiver structure
- Sensitivity to timing offsets
- Sensitivity to frequency impairments
- Sensitivity to frequency offsets
- OFDM symbol synchronisation
- Frequency synchronisation
- Phase / Amplitude recovery
- Channel estimation
- Pilot tracking
- Synchronisation for 802.16

OFDMA

- OFDMA advantages
- Full versus partial spectrum utilisation
- OFDMA versus MC-CDMA
- Frequency hopped OFDMA

802.20

- IEEE 802.20 PAR
- 802.20 modes of operation
- Comments from 802.16 group on 802.20
- 802.20 versus 802.16e
- 802.20 versus 3G
- 802.20 technology overview

Wireless / Mobile Channel Modelling

SYLLABUS

This course provides attendees with a solid and intuitive understanding of Microwave and Radio propagation fundamental and principles. The course covers radio propagation and its affects on the design of wireless systems for maximizing capacity and coverage as well as minimizing transmitted power and interference. Also the principles of signal fading and noise enhancement for both fixed and mobile systems will be considered. The effect of time varying and time dispersive properties of the channel are covered to characterize the received signal at the receiver.

The course will cover the use of wireless channel model in actual simulations which is ideal for engineers and researchers who have little or no knowledge of using standard complex MIMO channel models (such as SCM, LTE channel model) within simulations. The course covers existing standardised SISO/ MIMO channel model and there use within simulation environments.

The course will include:

- Radio propagation fundamentals and principles
- Propagation models and link budget
- Propagation in microwave terrestrial relay and satellite systems
- Channel fading and it affect on system design
- Understanding ITU and MIMO channel models
- Radio regulation and spectrum management
- Introduction of radio frequency planning tools (Radio Mobile)
- Fading and noise enhancement in fixed and mobile wireless systems
- Detailed understanding of integrating wireless channel model in actual simulation for both SISO/MIMO systems.
- Factor to be considered in the design, integration and simulation of propriety wireless channel model.
- Propagation channels and modelling in UHF spectrum

Wireless "Whitespace" Communications Design

SYLLABUS

This course provides attendees with a solid and intuitive understanding of the unused portion of UHF spectrum commonly referred to as white space. The course covers the regulation of radio spectrum and the technical aspects of cognitive white space networking. Recent advances in white space networking techniques and current industry developments will also be covered. The course will give a brief account of radio propagation and channel modelling in white space as well as covering the principles of prior planning and coordination between operator and regulator.

The course will include:

- Potential of White space networking
- Radio frequency regulation and working group (IEEE 802.22)
- Network planning, coordination and service requirements.
- Dynamic spectrum access in DTV whitespaces
- Case studies and past, present and future of white space networking
- Introduction of radio frequency planning tools (Radio Mobile)
- Characterization of white space (i.e. spatial/temporal variation and spectrum fragmentation)
- Spectrum sensing and assignment
- Cognitive networking challenges
- Coexistence of dual frequency networks
- Propagation channels and modelling in UHF spectrum

VHDL Simulation & Synthesis

SYLLABUS

Introduction to VHDL

- The origins of VHDL
- VHDL basics
- Benefits of VHDL
- VHDL levels of abstraction
- Abstraction and timing
- VHDL in the system design flow
- The VHDL design flow
- VHDL synthesis
- Modelling hardware in VHDL
- VHDL design entities
- Entity declarations
- Architectures
- Using libraries and packages
- Concurrent signal assignments
- Signal assignments with delays

Hierarchy in VHDL

- Component declarations
- Component instantiation
- Named port mapping
- Positional port mapping
- Direct instantiation
- Configuration specifications
- Entity binding
- Port modes
- VHDL processes
- Processes sensitivity lists
- Test benches

Objects and Data Types

- Objects in VHDL
- Constants, variables and signals
- VHDL types
- Scalar types
- Arrays
- Records
- Synthesis of ints and enums
- Custom types and subtypes
- Tristate and resolved types
- std_ulogic and std_logic
- unsigned and signed
- Attributes

Concurrent and Sequential Statements

- Concurrent statements
- Sequential statements
- Conditional & selective signal assignments
- The generate statement
- Signal and variable assignments
- Synthesis of statements
- Latch inference
- For loops & loop synthesis

Simulation and Synthesis

- How a VHDL simulator works
- Event driven simulation
- Event processing
- Simulation (delta) cycles
- Delta cycle race conditions
- Elaboration
- Process synthesis
- Synthesisable processes styles & templates
- Combinational logic in a process
- Synchronous (clocked) processes

Finite State Machines (FSMs)

- Review of Moore and Mealy state machines
- Finite state machines representation
- Use of enums to represent state
- FSM code structure
- FSM example (traffic light controller)
- FSM implementation example
- Synthesis of FSMs

Subprograms and Packages

- Subprograms
- Functions
- Procedures
- Differences between functions and procedures
- Subprogram declarations
- Packages
- Package declaration
- Package body
- Example: colour package

Configurable and Scalable Designs

- Generic parameters
- Generic mapping
- Example: generic wordlength
- Configuration declarations
- Default binding
- Example Configuration Declaration
- Assertions

Practical Exercises Undertaken During Course

- Introduction to Mentor Graphics ModelSim for VHDL simulation
- Introduction to Xilinx ISE for synthesis & implementation
- 2-bit adder design
- Loadable up-down counter
- Generating regular repetitive structures
- Finite impulse response filter
- Finite state machine
- Post synthesis + post place and route simulation
- RAM board model
- Direct Digital Synthesis (DDS)

Steepest Ascent Ltd., 94 Duke St, Glasgow G4 0UW, Scotland, UK
www.steepestascent.com

Technical Course Information

Course Targets
The intensive technical courses will present and examine the theory and use of algorithms, applications and architectures. The courses will feature the software design flow from concept, to bit true simulation, to actual hardware implementation.

Level
The level of the courses will include some initial review and revision. The style of the course and the hands-on labs sessions mean that this work is self-paced. There will be a number of experienced staff assisting Prof. Stewart during lab sessions making the course suitable for both new graduates and experienced engineers.

Course Presentation
DSP is often seen as an esoteric and very mathematical subject. In these courses, the necessary mathematical theory is presented on a "need to know basis" and in an intuitive style using both simulations and demonstrations. This presentation style and ethos has been presented with considerable success to many companies, both small and large, in both Europe and the USA.

Course Format
50%Lectures and presentation | 40% Workshop with software hands-on simulation | 10% Tutorial Discussion

Course Materials
All attendees will receive a comprehensive set of electronic and printed versions of the teaching materials. A DVD containing all the simulation models used during the course will also be distributed. The notes provided form a superset of the materials presented on the course and will allow further in depth study after the course.

Instructors
The courses will be led by the team of experienced design engineers from Steepest Ascent of Professor Bob Stewart. They have been successfully presented in Europe, United States and Asia. Prof Bob Stewart has extensive experience presenting industry DSP courses in the USA and Europe. He is currently a faculty member of the Department of Electronic and Electrical Engineering at the University of Strathclyde. Prior to joining the University of Strathclyde, Prof Stewart was a visiting professor in Dept of Electrical Engineering at the University of Minnesota in 1990, and a visiting scholar at the University of Southern California in 1986/7. Since 1997 he has been a part-time visiting professor at UCLA.

Services
Following services are included in the fee for the technical courses: participation at the course/workshop, catering during coffee breaks, soft drinks, lunch, and course documentation. The lectures are given in English.
The course hours are from 8.30 a.m. to 6.00 p.m.. The Munich course location is:
DERAG HOTEL and LIVING | Hotel Prinzessin Elisabeth
Geyerstrasse 52 | 80469 München | Germany
E-Mail: sales.pe@deraghotels.de | Phone: +49 89 72017 153 | Fax: +49 89 72017 160
http://www.deraghotels.de/en/PE.htm
The hotel has reserved a number of rooms. Please make your booking directly with the hotel referring to "qaqadu event gmbh". Further hotels are available through www.hrs.com.

On-site Courses
All short courses can also be offered on-site at companies in either a general or a customised form. If you have specific requirements please do not hesitate to contact us.

Terms and Conditions
Invoices have to be settled for participation. For a written cancellation within six weeks before course starts a fee of 200 € plus VAT per person is due. A deregistration within two weeks before the course will cost 50 % of registration fee plus VAT per person. For non-attendance or later notice the whole fee plus VAT per person will be charged. A substitute of the registered participant will be accepted. qaqadu event gmbh reserves the right to cancel or modify the course and place at short notice and will not accept liability for costs incurred by participants or their organisations for any expenses including cancelled travel arrangements and/or accommodation reservations. Neither qaqadu event gmbh nor Steepest Ascent is liable for failure if such failure is a result of Acts of God (Force majeure) and neither is obliged to reimburse the course fee. All fees exclude German state value added tax.

qaqadu event gmbh
Maximilianstraße 8
82319 Starnberg, Germany
T +49 8151 55 50 09 11
F +49 8151 55 50 09 10
E contact@qaqadu.com

Geschäftsführung:
Mandy Ahlendorf, Joachim Hüggenberg
HRB 173924, Amtsgericht München
TAX No. 117/135/50029 ID DE260317785
www.hightech-events.com

Kreissparkasse München Starnberg
Account 27007814 BLZ 702 501 50
IBAN DE67702501500027007814
SWIFT-BIC BYLADEM1KMS

Short courses are developed and presented by

www.steepestascent.com

Registration

This written registration is effective. The number of participants is limited. The invoice will be mailed with the registration confirmation. Registration deadline is ten workdays before course begin:

- via mail to qaqadu event gmbh, Maximilianstrasse 8, DE-82319 Starnberg – or –
- via fax to: +49-8151-55 50 09 10 – or –
- via E-Mail to contact@hightech-events.com

Terms and Conditions: Invoices have to be settled for participation. For a written cancellation within six weeks before course starts a fee of 200 € plus VAT per person is due. A deregistration within two weeks before the course will cost 50 % of registration fee plus VAT per person. For non-attendance or later notice the whole fee plus VAT per person will be charged. A substitute of the registered participant will be accepted. qaqadu event gmbh reserves the right to cancel or modify the course and place at short notice and will not accept liability for costs incurred by participants or their organisations for any expenses including cancelled travel arrangements and/or accommodation reservations. Neither qaqadu event gmbh nor Steepest Ascent is liable for failure if such failure is a result of Acts of God (Force majeure) and neither is obliged to reimburse the course fee. All fees exclude German state value added tax.

☐ Herewith, I (we) bindingly register for the following course. I accept the terms and conditions.

3 Day Courses	☐ € 1.850,00 regular fee
DSP Theory Algorithms & Architectures	☐ € 1.670,00 early registration until 70 days before course
☐ April 17-19, 2012 ☐ November 6-8, 2012	☐ € 1.570,00 per participant of two from the same company
DSP for FPGAs	☐ € 1.480,00 per participant of three or more from the same company
☐ May 22-24, 2012 ☐ October 9-11, 2012	☐ € 1.020,00 University Rate (Please enclose evidence.)

☐ Please inform us on the ______________________ course(s) in Scotland, UK and the US.

☐ We are interested in the ______________________ course(s) for on-site realization at our premises of ______________ (company) in ______________ (town, country).

Name(s) ______________________

Title / Position / Department ______________________

Company ______________________

E-mail address(es) ______________________

Telephone ______________________ Fax ______________________

I learned about this course from ☐ Invitation ☐ Colleagues ☐ Advertisement ☐ Trade Press ☐ Internet Search ☐ Other ______________

Billing address:

Company ______________________

Purchase Order No. ______________ VAT-ID-No. (for non-German EU only) ______________

Street / PO Box ______________________

Country-Zip Code-City ______________________

I prefer to pay by credit card: Credit Card No. ______________ Expiration Date _____/_____

Town, Date Signature ______________________

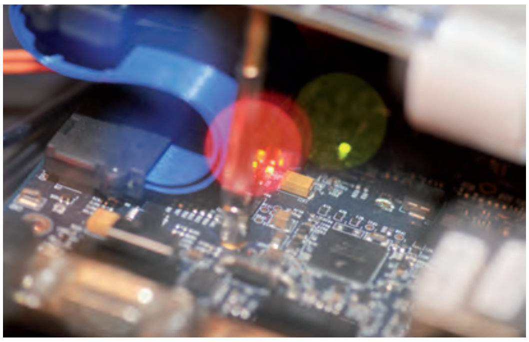
qaqadu event gmbh
Maximilianstraße 8
82319 Starnberg, Germany
T +49 8151 55 50 09 11
F +49 8151 55 50 09 10
E contact@qaqadu.com

Geschäftsführung:
Mandy Ahlendorf, Joachim Hüggenberg
HRB 173924, Amtsgericht München
TAX No. 117/135/50029 ID DE260317785
www.hightech-events.com

Kreissparkasse München Starnberg
Account 27007814 BLZ 702 501 50
IBAN DE67702501500027007814
SWIFT-BIC BYLADEM1KMS

MOST® FORUM

20 March 2012
Stuttgart/Esslingen (Germany)



ENTERTAINMENT
INFORMATION
MOBILE CONNECTIVITY
CONNECTED SERVICES
DRIVER ASSIST

INDUSTRY PROFESSIONALS AND ACADEMIA

TECHNOLOGY HIGHLIGHTS AND FUTURE OUTLOOK

MOST - One Network for Many Applications

Exhibitors:

Audi, BMW GROUP, DAIMLER, GÖPEL electronic, HAMAMATSU PHOTON IS OUR BUSINESS, K2L CONNECTING NETWORKS, Melexis Microelectronic Integrated Systems, MOST COOPERATION, RUETZ SYSTEM SOLUTIONS, SMSC SUCCESS BY DESIGN, Telemotive AG, TTTech, vector

Conference Program

09.30	Registration and Reception Coffee *Exhibition Opens*	
10.00	**Opening and Welcoming Speech** *Moderation: Henry Muyshondt, MOST Cooperation*	
10.05	**Keynote**	Keynote Speech
10.30	**New Physical Layer Based on All Glass Fiber (AGF) Solution** *Hayato Yuki / Kiyoshi Kato / Yuji Nakura / Tetsuji Tanaka, Sumitomo*	MOST Physical Layer
10.55	**Outlook on Next Generation MOST Physical Layer with 1 Gbit/s Keeping Today's Optoelectronics and Fiber** *Dr. Norbert Weber / Conrad Zerna, Fraunhofer IIS*	
11.10	**High Speed Modulation of Green Lasers and LED** *Prof. Dr. Olaf Ziemann / Juri Vinogradov / Sven Loquai, Georg-Simon-Ohm University of Applied Sciences Nuremburg*	
11.25	**New MOST Optical Connector** *Naoshi Serizawa, Yazaki*	
11.40	Exhibitor Presentations	
12.00	Lunch / Networking / Exhibition	
13.45	**MOST150 Compliance Testing - Challenges and Test Strategies** *Alle Pavan / Patro Gajendra Kumar / Ghislain Simon, Tektronix*	MOST Compliance and Quality
14.00	**All in One – Data Logging Without Compromise** *Marjan Hanc, TTTech Automotive*	
14.15	**Reliability Analysis of a MOST Based Advanced Driver Assistance System Using Virtual Prototypes** *Dr. rer. nat. Oliver Bringmann, Sebastian Reiter, Prof. Dr. rer. nat. Wolfgang Rosenstiel, FZI*	
14.30	**MOST in Driver Assistance** *Dr. Wolfgang Bott, MOST Cooperation*	MOST Network and System Architecture
14.45	**How to Guarantee Application Functionality in a MOST150 Network - An Embedded Systems Approach** *Friedrich Schick / Walid El Kassem, X2E; Prof. Dr.-Ing. Norbert Wehn, University Kaiserslautern*	
15.00	**Vehicle Access for Mobile Devices Using MOST Framework** *Joachim Leonhard, K2L*	
15.15	Coffee Break / Networking / Exhibition	
16.15	**Digital Content Protection on MOST** *Jochen Klaus-Wagenbrenner, HARMAN*	MOST Network and System Architecture
16.30	**IP Architecture in a MOST Based Infotainment System** *Dr. Alexander Leonhardi / Uwe Walter / Rico Hauke, Daimler AG*	
16.50	**MOST - The Versatile Automotive Backbone on its Way into the Future** *Harald Schoepp, SMSC*	
17.10	Conclusion and End of Conference *Exhibition Closes*	

Welcome to the MOST Forum

MOST Forum invites you to Stuttgart/Esslingen, Germany, to the one-day congress with numerous specialists presenting the latest and future innovations on MOST based infotainment technology. The conference will provide a forum for a broad audience from the automotive electronics industry and academia reaching from researchers, designers, engineers, system developers, to purchasers and journalists, and to the managers of the industries involved.

Speakers

Dr. Wolfgang Bott	*MOST Cooperation*
Dr. rer. nat. Oliver Bringmann	*FZI (Research Center for IT)*
Marjan Hanc	*TTTech Automotive*
Rico Hauke	*Daimler AG*
Yuji Nakura	*Sumitomo*
Walid El Kassem	*X2E*
Kiyoshi Kato	*Sumitomo*
Jochen Klaus-Wagenbrenner	*HARMAN*
Patro Gajendra Kumar	*Tektronix*
Dr. Alexander Leonhardi	*Daimler AG*
Sven Loquai	*Univ. of Appl. Sc. Nuremburg*
Alle Pavan	*Tektronix*
Sebastian Reiter	*FZI (Research Center for IT)*
Prof. Dr. rer. nat. Wolfgang Rosenstiel	*FZI (Research Center for IT)*
Friedrich Schick	*X2E*
Harald Schoepp	*SMSC*
Naoshi Serizawa	*Yazaki*
Ghislain Simon	*Tektronix*
Tetsuji Tanaka	*Sumitomo*
Juri Vinogradov	*Univ. of Appl. Sc. Nuremburg*
Uwe Walter	*Daimler AG*
Dr. Norbert Weber	*Fraunhofer IIS*
Prof. Dr.-Ing. Norbert Wehn	*University Kaiserslautern*
Hayato Yuki	*Sumitomo*
Conrad Zerna	*Fraunhofer IIS*
Prof. Dr. Olaf Ziemann	*Univ. of Appl. Sc. Nuremburg*

Marketing

There are additional opportunities to be recognized by the top professionals from the automotive electronics industry by sponsoring the conference or placing an ad in the Elektronik automotive special edition accompanying the MOST Forum 2012.



Location

Neckar Forum
Ebershaldenstrasse 12
73728 Esslingen/Neckar, Germany

T +49 711 41111 700
F +49 711 41111 999
W www.neckar-forum.com

Accommodation

For accommodation, a special rate of 120 Euro (per night and person, incl. VAT) will be available at the Best Western Premier Hotel Park Consul Stuttgart/Esslingen.

Best Western
Premier Hotel Park Consul
T +49 711 41111 0
F +49 711 41111 699
E pcesslingen@consul-hotels.com
W www.pcesslingen.consul-hotels.com

Accommodation is also available through HRS booking service.

Directions

By car
Coming from the direction of Karlsruhe, take the Esslingen exit to Esslingen onto the B 10 towards Stuttgart, take the Esslingen-Zentrum exit, follow the Altstadtring aiming for Neckar Forum.
Coming from the direction of Munich, take the Wendlingen exit to Esslingen via the B 313 onto the B 10, take the Esslingen-Zentrum exit, follow the Altstadtring aiming for Neckar Forum.

Distance by car:
From Stuttgart: app. 20 minutes
From Frankfurt Airport: app. 2 hours
From Munich: app. 2.5 hours

By train
Take the train to Esslingen Railway Station, from there take a taxi (5 minutes).

Distance by train:
From Stuttgart: app. 20 minutes
From Frankfurt Airport: app. 2 hours
From Munich: app. 2.5 hours

By plane
From Stuttgart Airport take a taxi (20 km, app. 25 minutes).

Further details are available at: www.mostforum.com/location/

Registration

The MOST Forum is looking forward to welcoming you to Stuttgart/Esslingen, Germany, to this one-day international MOST Conference and Exhibition with numerous specialists presenting the latest and future technologies and applications on MOST based infotainment technology:

The registration fee includes:

- Entrance to all conference sessions and exhibition at the MOST Forum on March 20, 2012
- Conference Proceedings
- Refreshments
- Buffet lunch

Please register by March 6, 2012, by sending this form via mail, fax or e-mail to:
qaqadu event gmbh I Maximilianstrasse 8 I 82319 Starnberg I Germany
T +49 8151 555009 11 I F +49 8151 555009 10
E contact@mostforum.com I W www.mostforum.com

Herewith I/we register for the MOST Forum on March 20, 2012 in Stuttgart/Esslingen. I accept the terms and conditions.

- ☐ Early Registration by December 31, 2011: 169 Euro
- ☐ Regular: 249 Euro
- ☐ Members of the MOST Cooperation: Free
  - ☐ I will attend the cocktail reception on March 19, 2012.
  - ☐ I will attend the All Members Meeting on March 20, 2012.
- ☐ University faculty and students: 49 Euro (Please include details of eligibility.)
- ☐ Speakers, members of the program committee and press: Free
- ☐ Sponsors: 3 free passes

Company/Institution:

Attendant: Ms./Mr. 1st Name: Last Name:
Position/Department:
Telephone: E-Mail:
City, Date: Signature:

Attendant: Ms./Mr. 1st Name: Last Name:
Position/Department:
Telephone: E-Mail:
City, Date: Signature:

Attendant: Ms./Mr. 1st Name: Last Name:
Position/Department:
Telephone: E-Mail:
City, Date: Signature:

Please send the invoice to:

Company/Institution
VAT-ID-No. (for non-German EU only)
Street Address / PO box
Country - Zip Code - City
I/we prefer to pay by credit card:
Credit Card No.
Cardholder Expiration Date /

Terms and Conditions: All fees exclude German VAT. This written registration is effective. The number of participants is limited. The invoice will be mailed a few weeks prior to the event. Invoices have to be settled for participation. A written cancellation is free before January 20, 2012. A deregistration within four weeks before the MOST Forum will cost 50 %. For non-attendance and late notice the whole fee plus VAT per person will be charged. A substitute of the registered participant will be accepted. The qaqadu event gmbh reserves the right to cancel or modify the MOST Forum and place at short notice and will not accept liability for any costs incurred by participants or their organisations including but not limited to cancelled travel arrangements and/or accommodation reservations. The event will be documented with photos and videos that will be published in various media. The participant agrees to his pictures being used for marketing and public relations purposes.

Conference Location

Neckar Forum
Ebershaldenstrasse 12
73728 Esslingen/Neckar
Germany
T +49 711 41111 700
F +49 711 41111 999
W www.neckar-forum.com

For more information on the MOST Forum please see www.mostforum.com or contact us:

MOST Forum
Mandy Ahlendorf
T +49 8151 55500911
E contact@mostforum.com
W www.mostforum.com

The MOST Forum is presented by qaqadu event gmbh.

qaqadu event gmbh
Maximilianstrasse 8
82319 Starnberg
Germany